



Power Distribution Network Design for VLSI

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A hands-on troubleshooting guide for VLSI network designers

The primary goal in VLSI (very large scale integration) power network design is to provide enough power lines across a chip to reduce voltage drops from the power pads to the center of the chip. Voltage drops caused by the power network's metal lines coupled with transistor switching currents on the chip cause power supply noises that can affect circuit timing and performance, thus providing a constant challenge for designers of high-performance chips.

Power Distribution Network Design for VLSI provides detailed information on this critical component of circuit design and physical integration for high-speed chips. A vital tool for professional engineers (especially those involved in the use of commercial tools), as well as graduate students of engineering, the text explains the design issues, guidelines, and CAD tools for the power distribution of the VLSI chip and package, and provides numerous examples for its effective application.

Features of the text include:

- * An introduction to power distribution network design
- * Design perspectives, such as power network planning, layout specifications, decoupling capacitance insertion, modeling, and analysis
- * Electromigration phenomena
- * IR drop analysis methodology
- * Commands and user interfaces of the VoltageStorm(TM) CAD tool
- * Microprocessor design examples using on-chip power distribution
- * Flip-chip and package design issues
- * Power network measurement techniques from real silicon

The author includes several case studies and a glossary of key words and basic terms to help readers understand and integrate basic concepts in VLSI design and power distribution.

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